Claims

1. Circuit configuration for voltage supply of a two-wire sensor (S) which is connected to a supply voltage source (U) via a first connection line (V1) in which a voltage longitudinal controller (SR) is positioned, and a second connection line (V2), wherein the controller output is connected to the second connection line (V2) via at least one limiting diode (D1), and wherein a current-limiting resistor (R1) is positioned in one of the two connection lines (V1) between the two-wire sensor (S) and the limiting diode (D1), characterized in that the controller output is connected to the second connection line (V2) via a series circuit comprising two limiting diodes (D1, D2), and that the joint node of the two limiting diodes (D1, D2) is connected to the control input of the voltage longitudinal controller (SR).

2. Circuit configuration as defined in Claim 1, characterized in that the two-wire sensor (S) is fitted with a so-called HART® interface, and a HART® resistor is positioned in one of the two connection lines (V1, V2).

3. Circuit configuration as defined in Claim 1 or 2, characterized in that a pole of the supply voltage source (U) is connected to an input of two-wire sensor (S) via a HART® resistor (RH), the drain source path of a field effect transistor (T1), and the current-limiting resistor (R1), the other input of which sensor is connected to the other pole of the supply voltage source (U) via the second connection line (V2) that the HART® resistor (RH), the drain source path of the field effect transistor (T1) and the current-limiting resistor (R1) are positioned in the first connection line (V1), that the source electrode of the field effect transistor (T1) is connected to the second connection line (V2) via a series circuit comprising a first and second limiting diode (D1, D2), that a first resistor (R4) is positioned parallel to the second limiting diode (D2), that the joint

node of the second limiting diode (D2) and the first resistor (R4) is connected to the base of a transistor (T2), the collector of which is connected to the gate electrode of field effect transistor (T1) via a second resistor (R3), and the emitter of which is connected to the second connection line (V2), and that the gate electrode of the field effect transistor (T1) is connected to the source electrode via a third resistor (R2).

4. Circuit configuration as defined in Claim 3, characterized in that at least one additional limiting diode each (D3, D4, D5, D6) is connected parallel to each limiting diode (D1, D2).

5. Circuit configuration as defined in one of the preceding claims, characterized in that the series connected limiting diodes (D1 through D6) are oppositely poled.